

FIG. 2

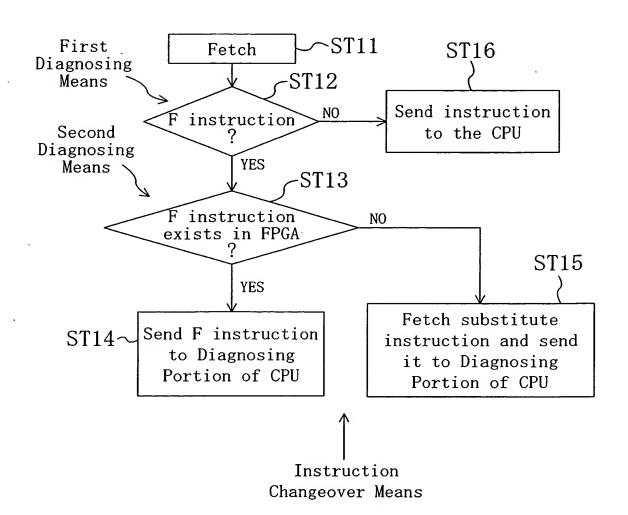


FIG. 3

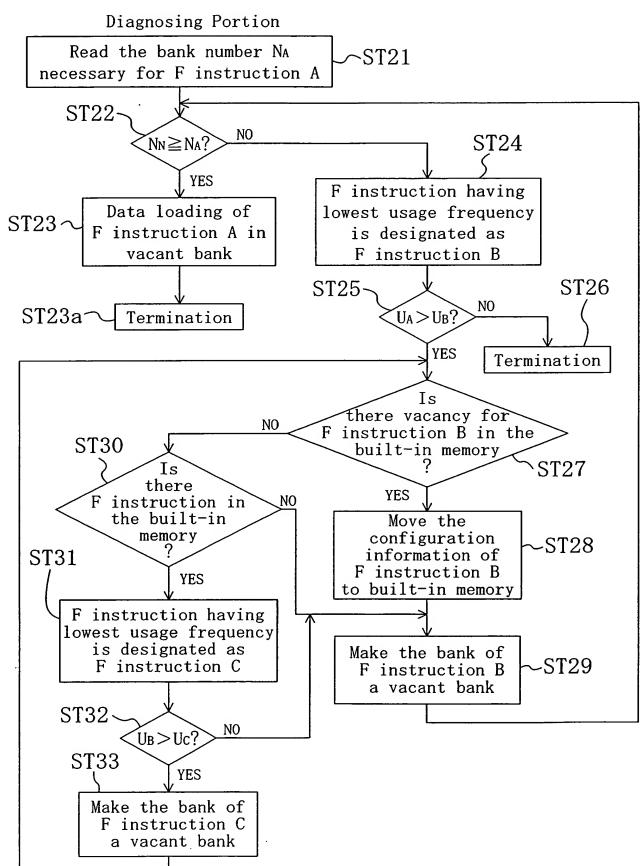


FIG. 4

Instructions		Comment		
ADD	D1, D2	#D1+D2→D2		
LSR	D3, D2	#D2 (D3)bit shift-right→D2		

FIG. 5

Bank0 ID=1		1					4
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FIG. 6A

FPGA 1 D1, D2, D3 #D1+D2 (D3)bit shift-right→D2

FIG. 6B

ADD D1, D2

#D1+D2→D2

LSR D3, D2

#D2 (D3)bit shift-right→D2

**FPGAend** 

# Termination of substitute instruction

## FIG. 7

Both F instruction and substitute instruction are described.

FPGA 0 D1, D2, D3 (addr) #D1+D2 (D3)bit shift-right→D2

#In case F instruction is executed, skip to (addr)

ADD D1, D2  $\#D1+D2 \rightarrow D2$ 

Substitute instruction from here

LSR D3, D2 #D2 (D3)bit shift-right→D2 Substitute

instruction up to this point

(Next instruction) # This is the address shown by (addr)

FIG. 8

ADD D1, D2  $\#D1+D2 \rightarrow D2$ 

LSR D3, D2 #D2 (D3) bit shift-right $\rightarrow$ D2

## FIG. 9

ID	Instruc-	Corresponding Configuration	Number of Ban	l. a
	tions	Data	Number of ban	banks

## FIG. 10

1	ADD D1, D2	Corresponding Configuration	. 1
1	LSR D3, D2	Data	1

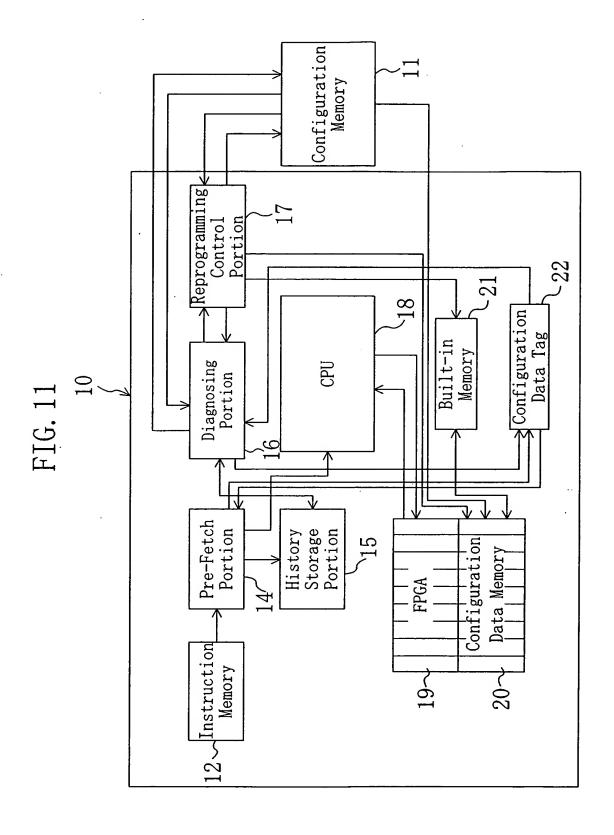


FIG. 12

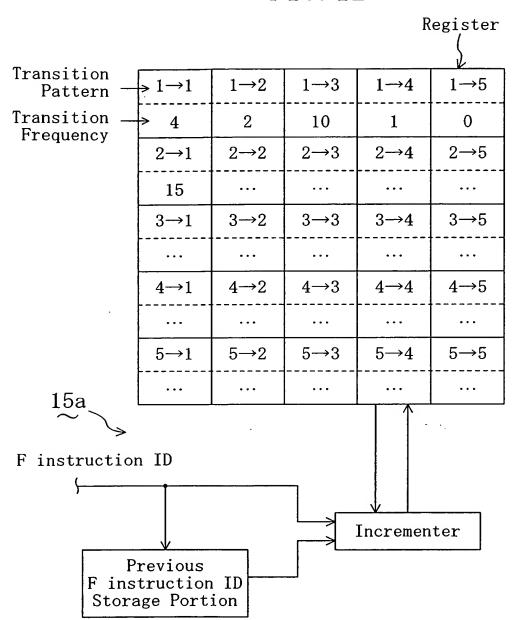


FIG. 13

